Image Processing System with a New Systolic Array LSI

Akira Ichinose, Kenji Suzuki, Yoshinori Wakimoto, Mitsuru Yanagisawa, Yuichiro Asano

Synopsis :

# Image Processing System with a New Systolic Array LSI*

*Synopsis:*

image is insufficient to handle all applications. An

user of an image processing board employing such an LSI can obtain high performance, until the limit of the array size is reached. Once this limit is exceeded, however, performance suddenly drops. As a result,

Table 1　LSI function list

One-dimensional convolution

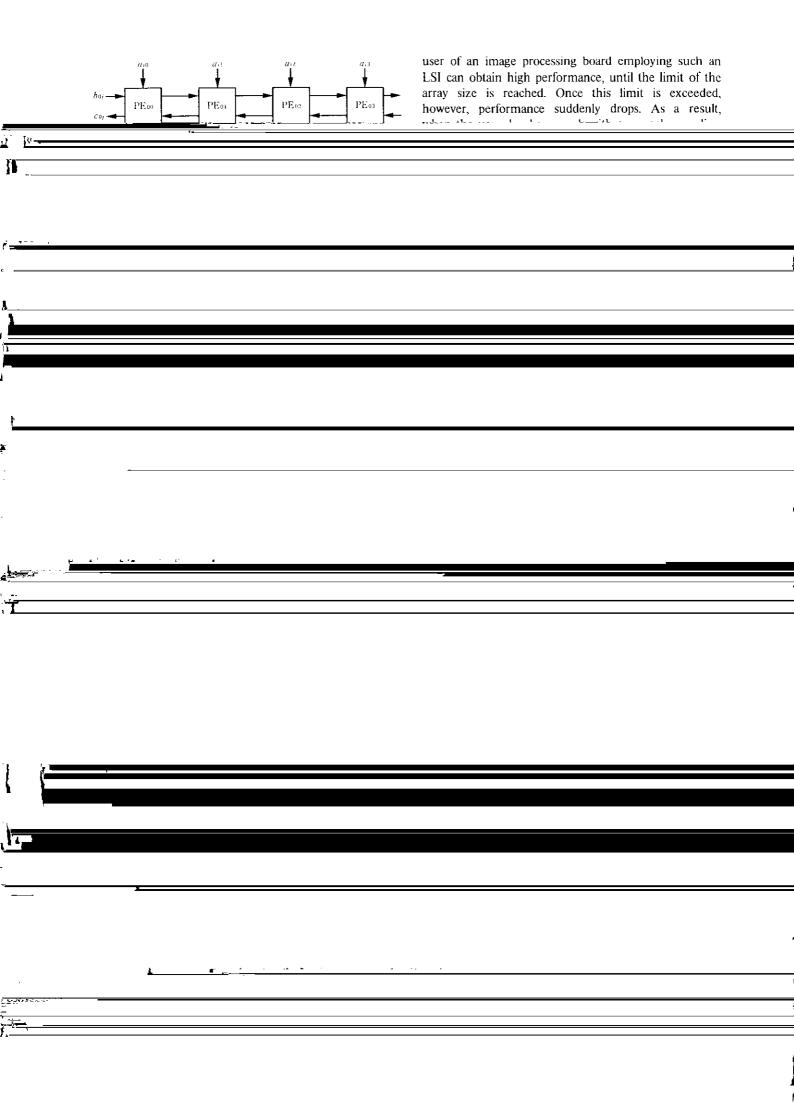Two-dimensional convolution

Matrix-vector multiplication
Gray scale transformation with look-up table

previous processing. The processing proceeds as follows: (1) The image data are read from a memory block;

array to carry out the convolution operation; (4) the

| 3 × 3 | 2 000 | 6.6 | 13.1 | 13.1 | 6.6 |

a WS, control is transferred to Dr. IMAGE II. The LSI

Table 3   Hardware component function list

tical, the architecture could be simplified and independent operation of Dr. IMAGE II became possible. Communication between the WS and Dr. IMAGE II are

Dr. IMAGE II, which has the following features:

(1) The image size and kernel size are variable so that a