

KAWASAKI STEEL TECHNICAL REPORT

No.30 (August 1994)

Special Issue on LSI

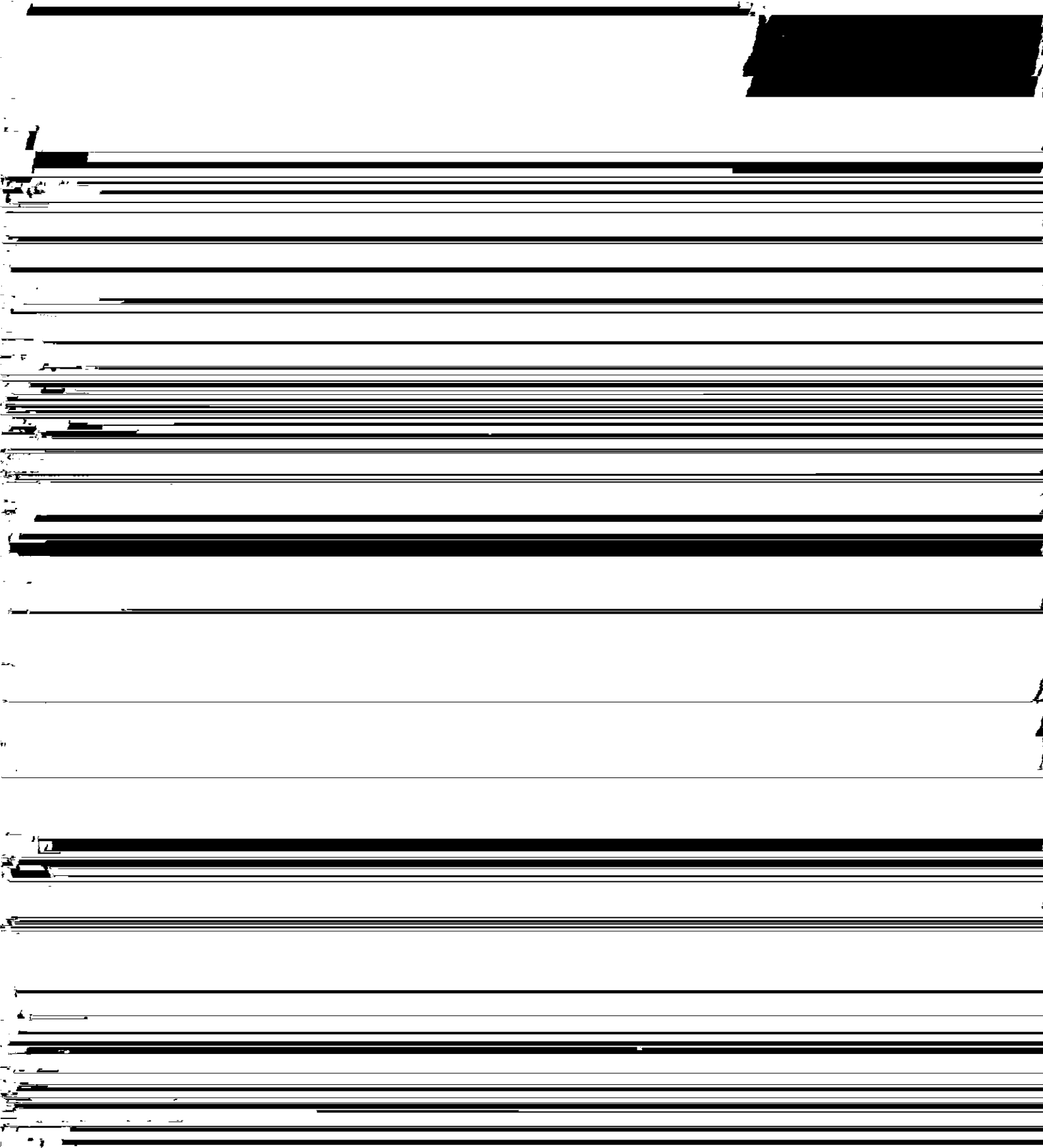
0.8-micron CMOS ASCPs

Hisaya Keida, Hiroyuki Hayashi, Kyo-ichi Kissei

0.8-micron CMOS ASCPs*

Synopsis:

The 0.8-micron double-layer metal CMOS (1.5- μ m)



test pattern development time increases proportionally to the third and fourth power of any gate count.²⁾ From the foregoing, it is obvious that unless test pattern generation is somehow automated and facilitated

3 Technology of 0.8- μ m ASCPs

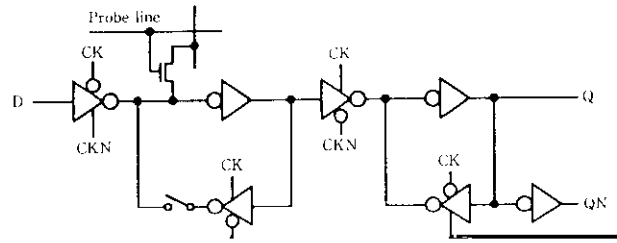
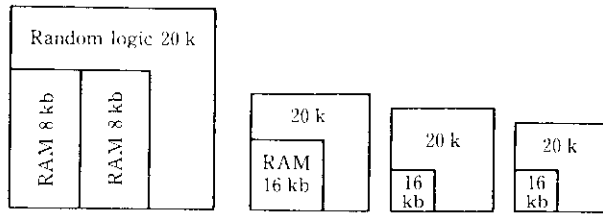
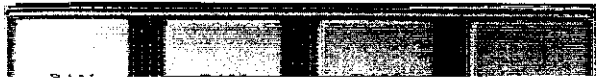


Fig. 4. Area comparison between Kawasaki Steel



The KG2H, KE2H, and KS2H series have scan registers uniquely structured on the chip to realize boundary





5 Conclusions