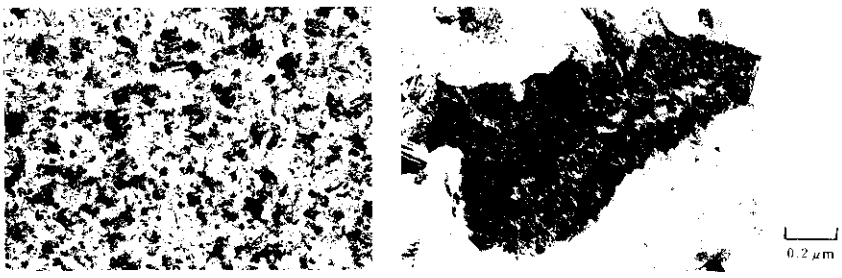
KAWASAKI STEEL TECHNICAL REPORT
No.30 (August 1994)
Special Issue on LSI

Improving Gate Oxide Integrity in p⁺pMOS Devices by



Synopsis:

The effect of polysilicon grain size on gate oxide integrity in BF_2 implanted polysilicon gate pMOS devices was investigated by measuring the electrical characteristics of a



(a) Conventional polysilicon (b) Large-grain polysilicon

Photo 1. TEM plan views of the polysilicon film

average grain sizes of conventional polysilicon (small grain) and large grain polysilicon are on the order of 0.05 μm and 1.0 μm, respectively. The undoped polysilicon gate, the gate oxide shows low-voltage (below 2 V) breakdown. The oxide defect density was calculated to be as high as 7.6 cm^{-2}. This infe

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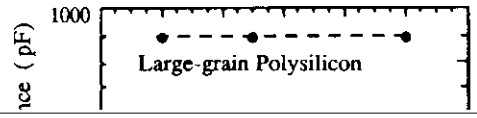
Photo 2 Dark-field TEM micrographs

capacitors as shown in Fig. 3. Q_{bd} at 50% failure with the large grain polysilicon gate capacitor is twice as large as that in the conventional polysilicon type. The use of



static CV measurement, and C_{inv}/C_{ox} is a parameter which is related to the carrier concentration in the polysilicon. C_{inv}/C_{ox} shows little difference in the two types of polysilicons. However, the C [illegible] of large grain polysili-

con gate MOS capacitors differs from that of conventional polysilicon gate MOS capacitors. Large grain polysilicon gate suppress the decrease in gate oxide capacitance and inversion capacitance.

The effect of polysilicon grain size and morphology

References

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