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New Products & Technologies

0.8 μm CMOS High Density Gate Array "KZ2H"*

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1 Product Profile

actual circuits are relatively small and, in many cases, the transistor sizes of conventional gate arrays were too

Table 1 Specifications of KZ2H family

Process	0.8μm CMOS double layer metal
Delay time[a]	0.27 ns
Max. usable gates	460 K gates
Voltage	5 V ± 10% 3.3 V ± 0.3 V 3 V ± 10%
Power dissipation[b]	3.1 μW/MHz/gate

[a] Power 2NAND, FO=2, Al=2mm
[b] 2NAND, FO=2, Al=0.34mm

(Relative value, %)

	SOG		Standard cell
	KZ2H	KG2H	KS2H
Density	100	~50	~80
Speed	100	~70	~90
Power	100	~160	~110

head associated with the KG2H and KS2H resulting from inclusion of the CrossCheck test function, the

ance equivalent to those of standard cells are required while maintaining a short TAT to ensure a satisfactory

facilitate this arrangement, tools such as a base array compiler are available for the KZ2H.

4.2 Libraries

For the KZ2H series, about 350 macro cells with approximately 150 functions are available. One function is provided with up to four levels of driving strength, so that a trade-off can be selected for each cell with respect to its area and speed

Table 4 Specifications of KZ2H SRAM's

	1-port asynchronous SRAM	2-port asynchronous SRAM	1-port synchronous SRAM
No. of R/W ports	1 R/W	2 R/W	1 R/W
Max. No. of bits	18 K	9 K	36 K
Word range	64～2 K	32～1 K	64～2 K
Bit range	1～36	1～36	1～36